OBLON, SPIVAK, ET AL
DOCKET #: 205086US2S
INV: Koichi OTAKE, et al.
SHEET 1 OF 10

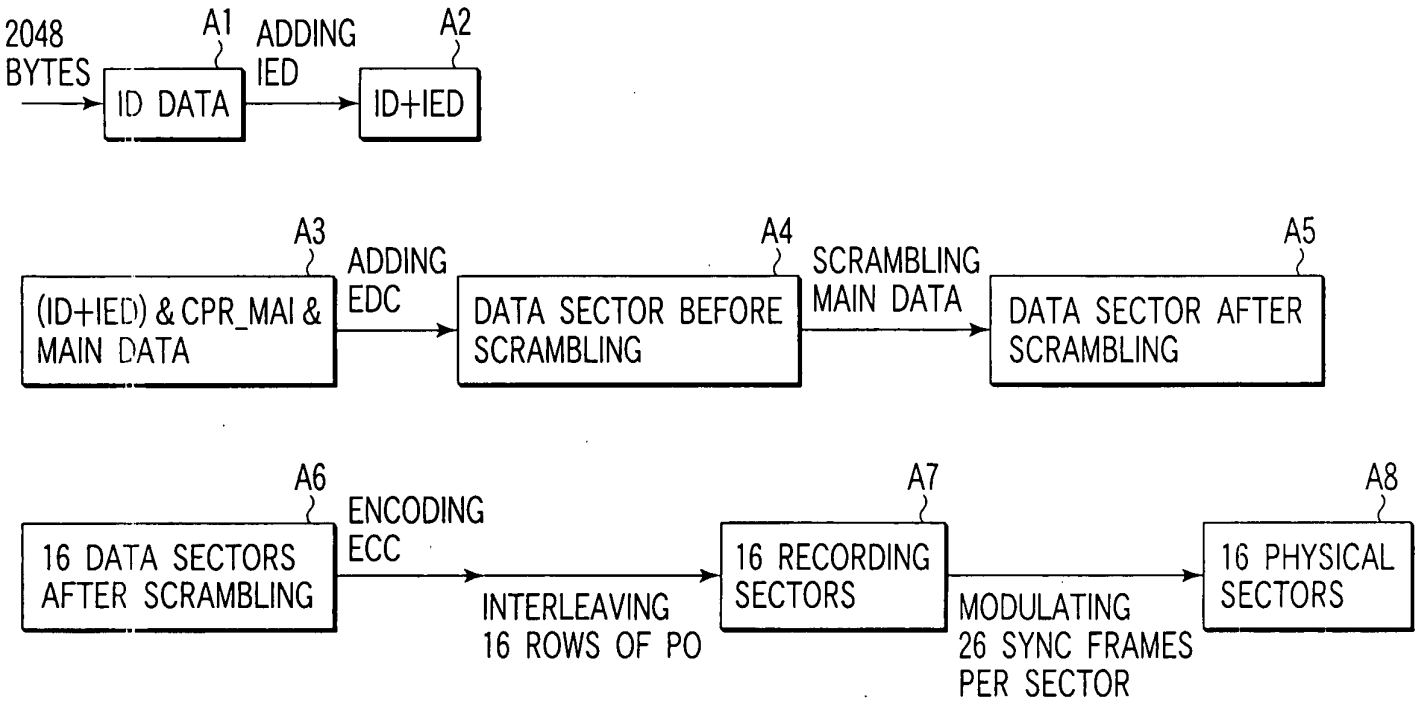

FIG. 1

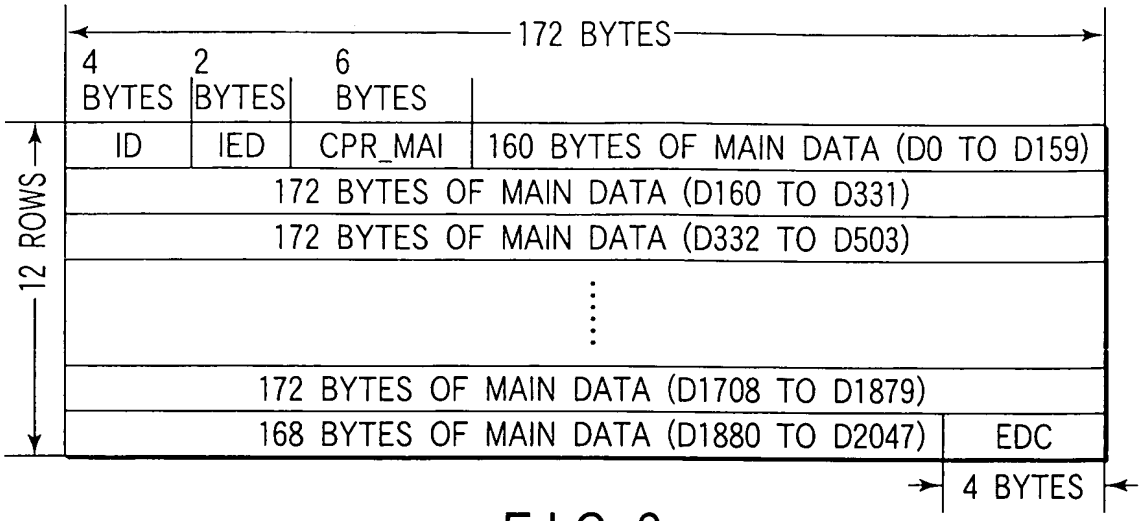

FIG. 2

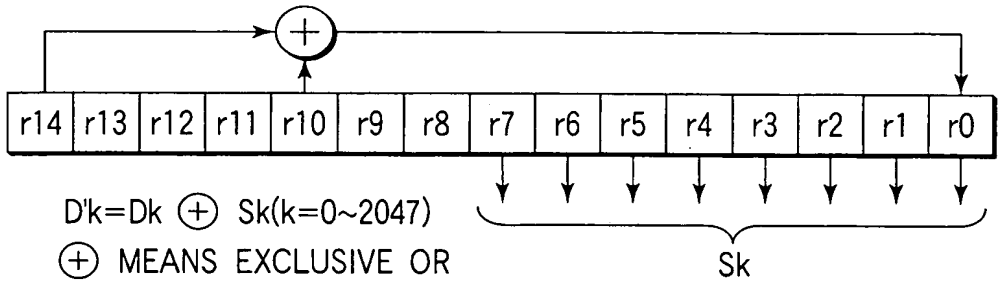

FIG. 3

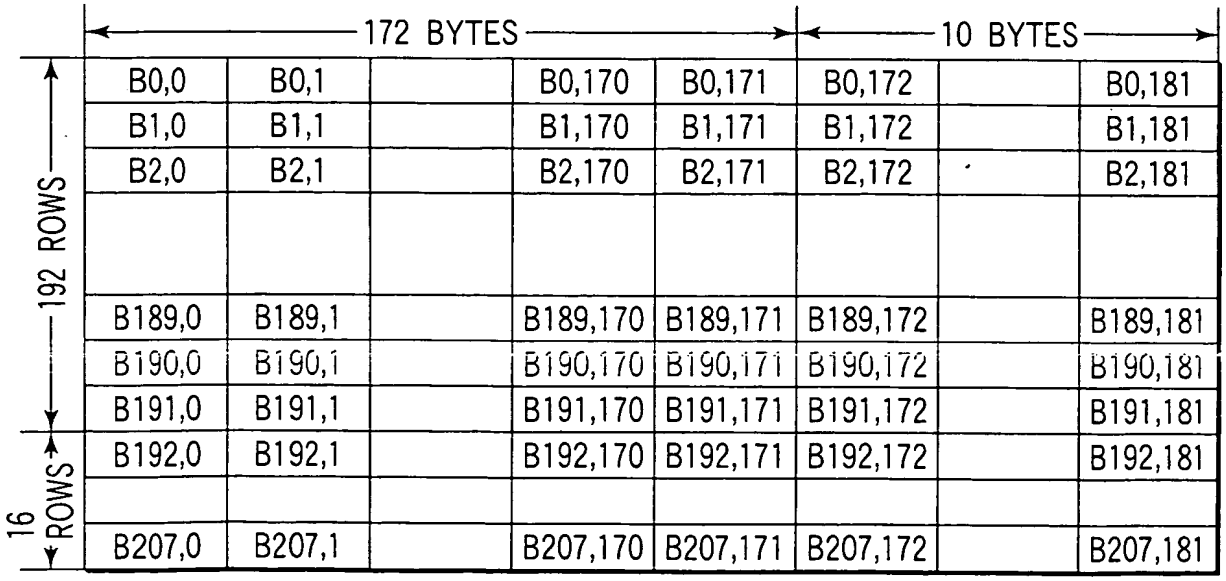

FIG. 4

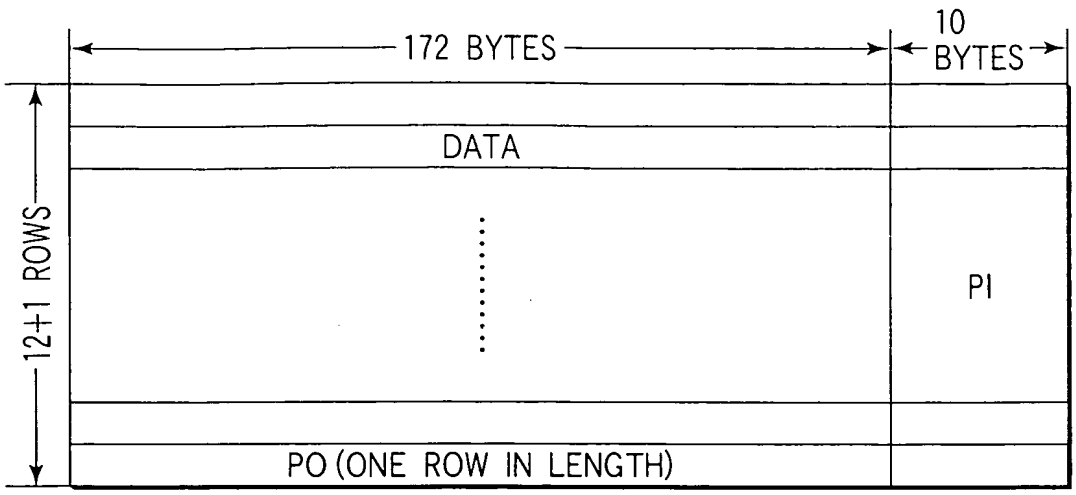
172 BYTES
10 BYTES
DATA
12+1 ROWS
PI
PO (ONE ROW IN LENGTH)

FIG. 5

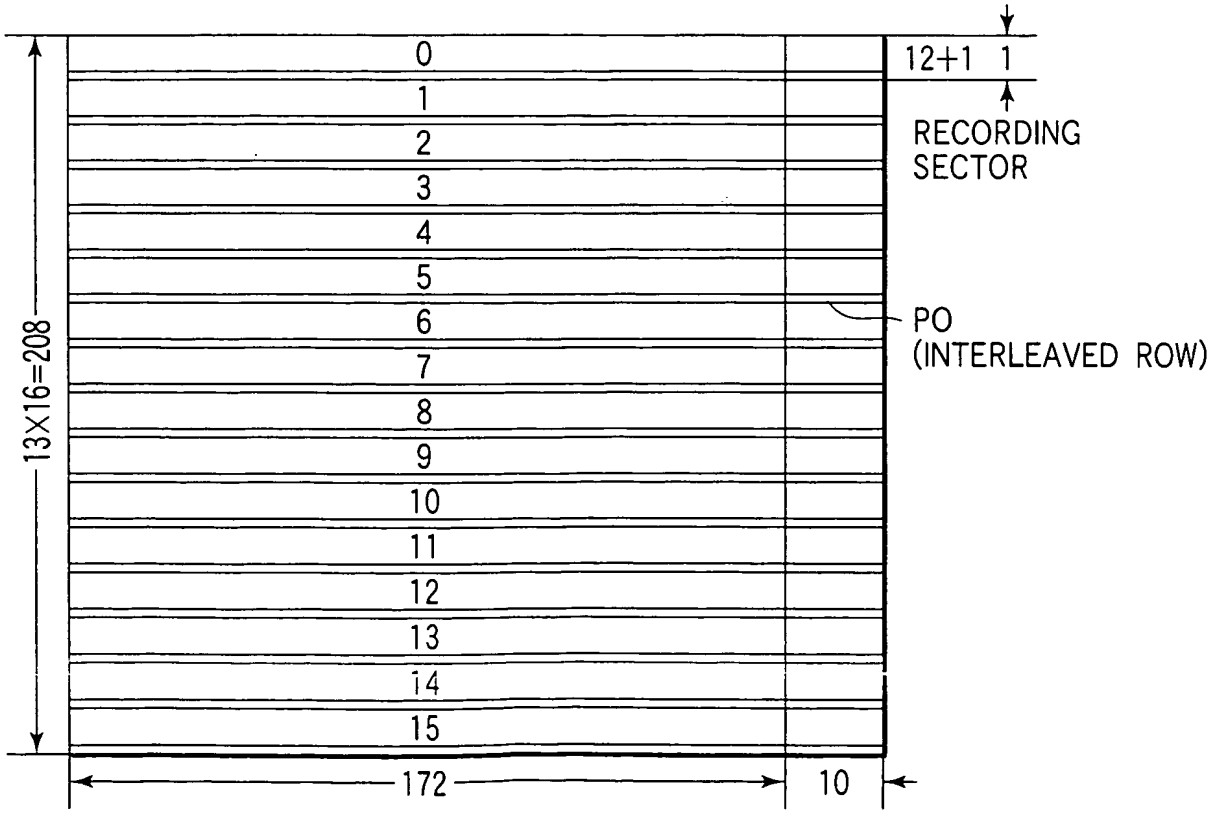
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
13X16=208
12+1
1
RECORDING SECTOR
PO
(INTERLEAVED ROW)
172
10

FIG. 6

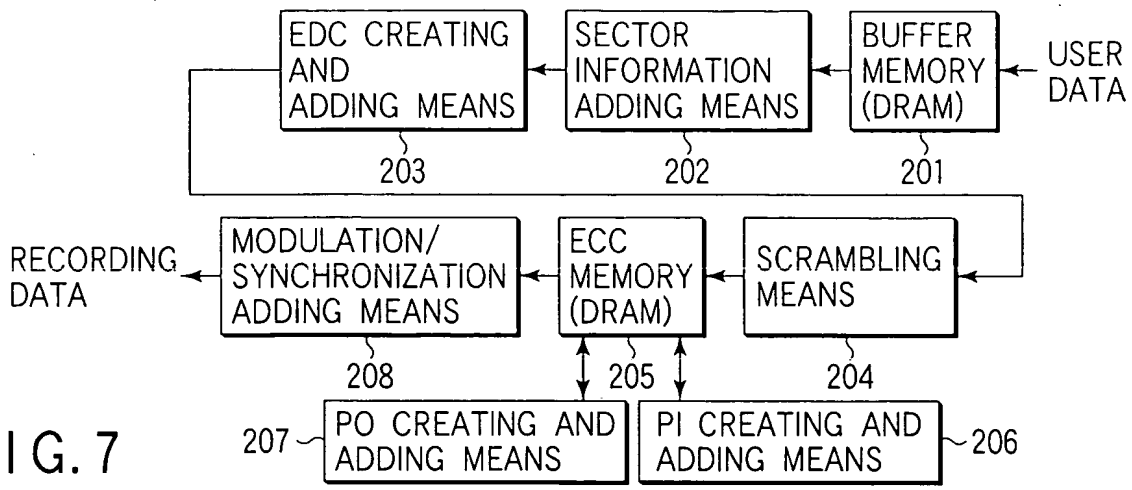

FIG. 7

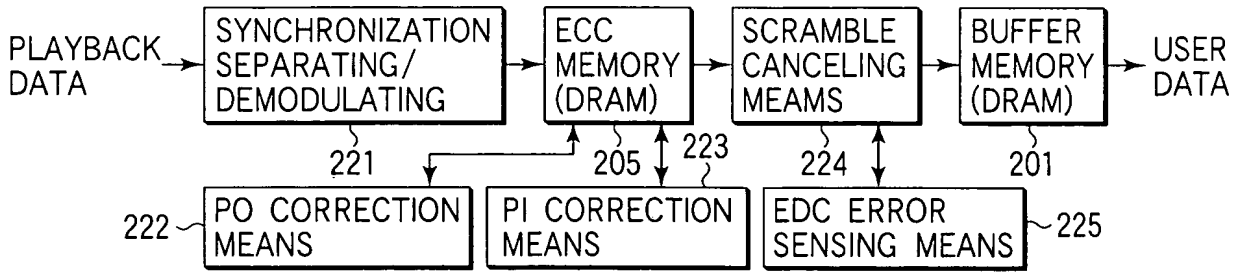

FIG. 8

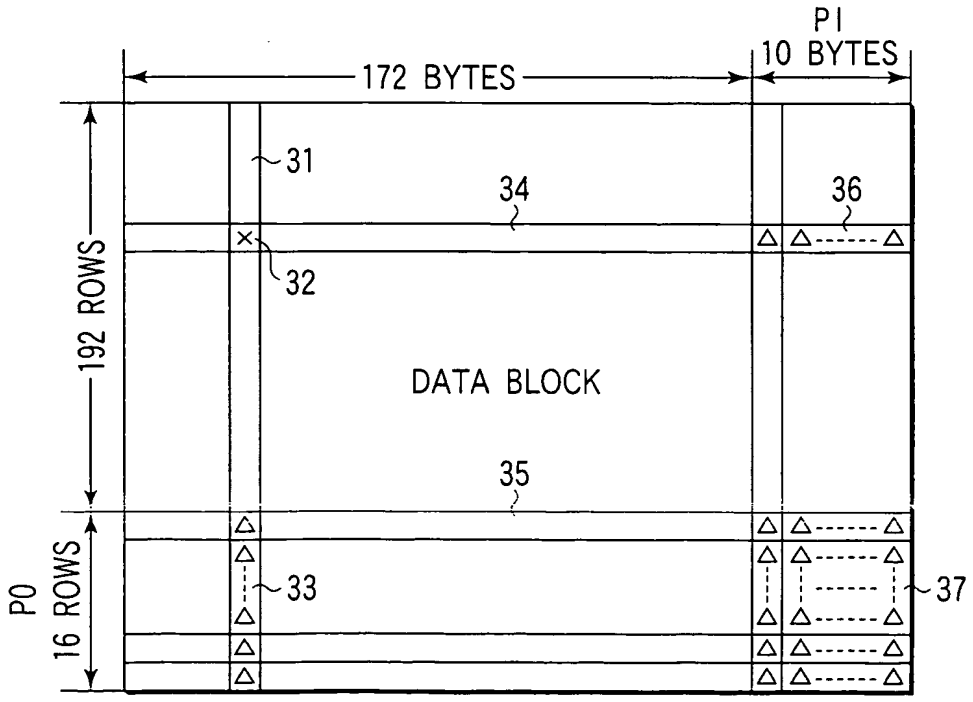

FIG. 9

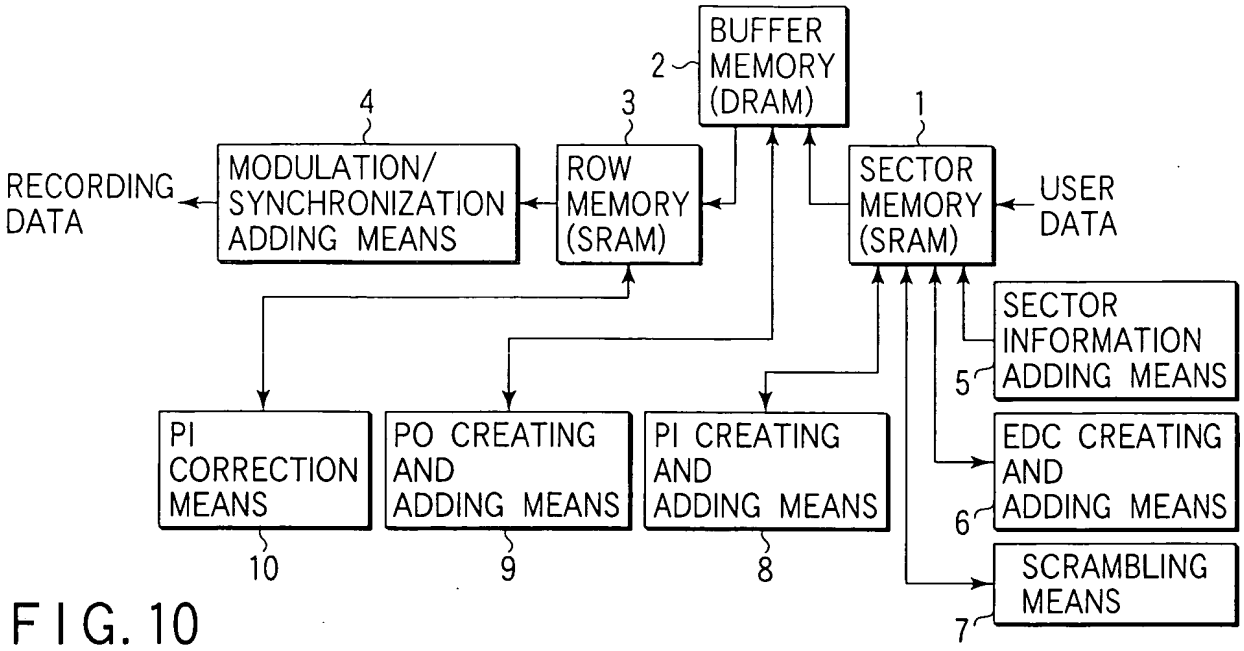

FIG. 10

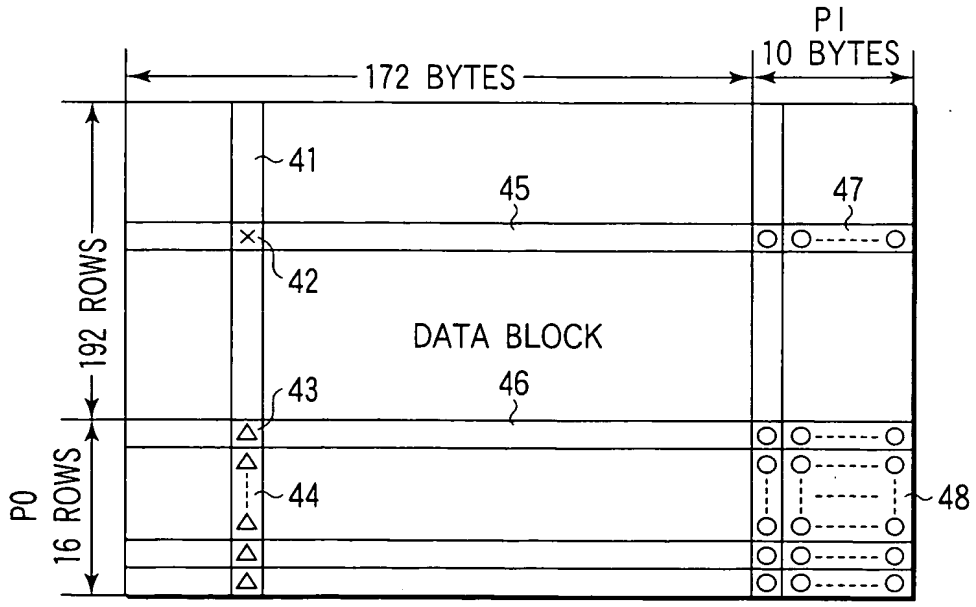

FIG. 11

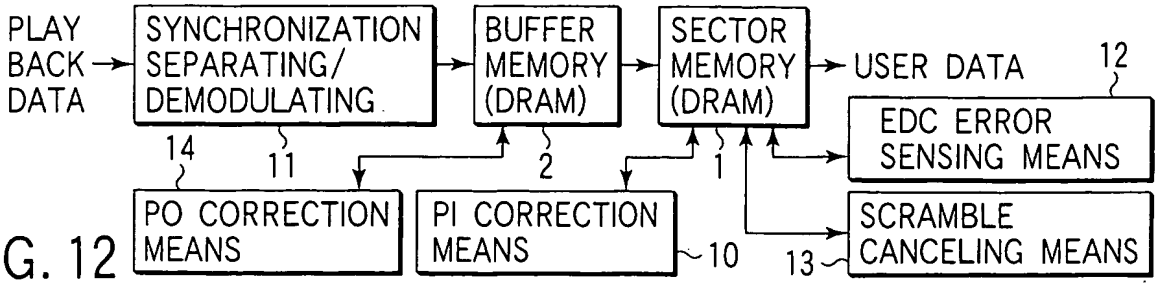

FIG. 12

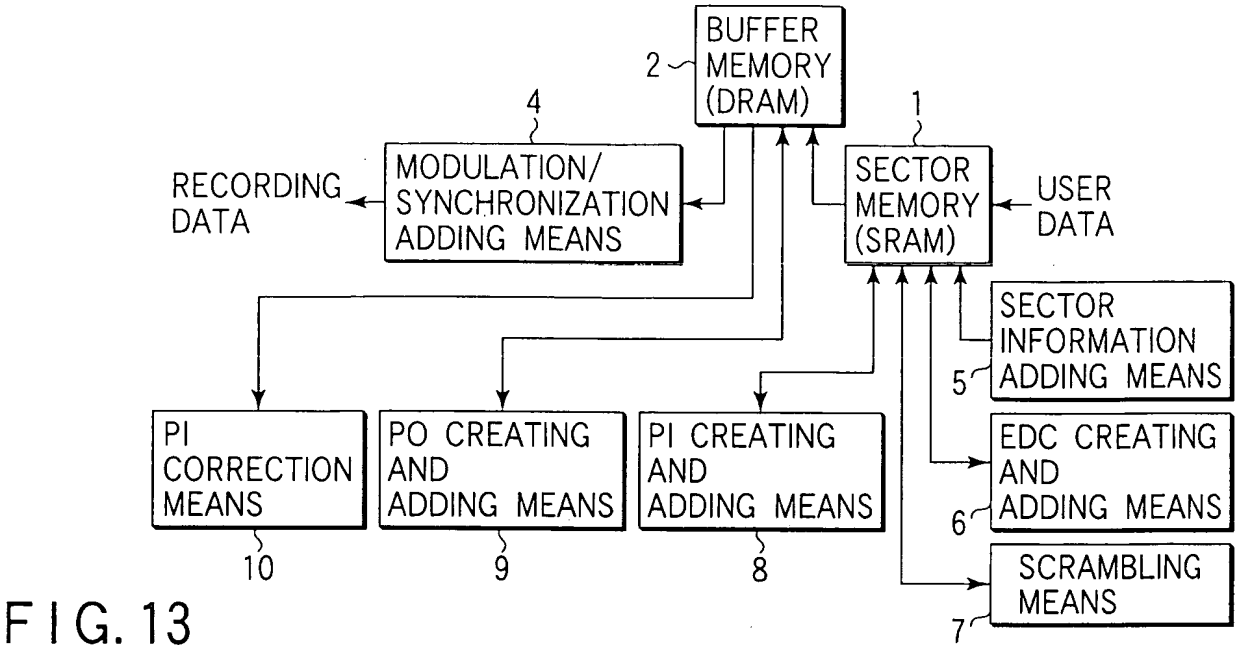

FIG. 13

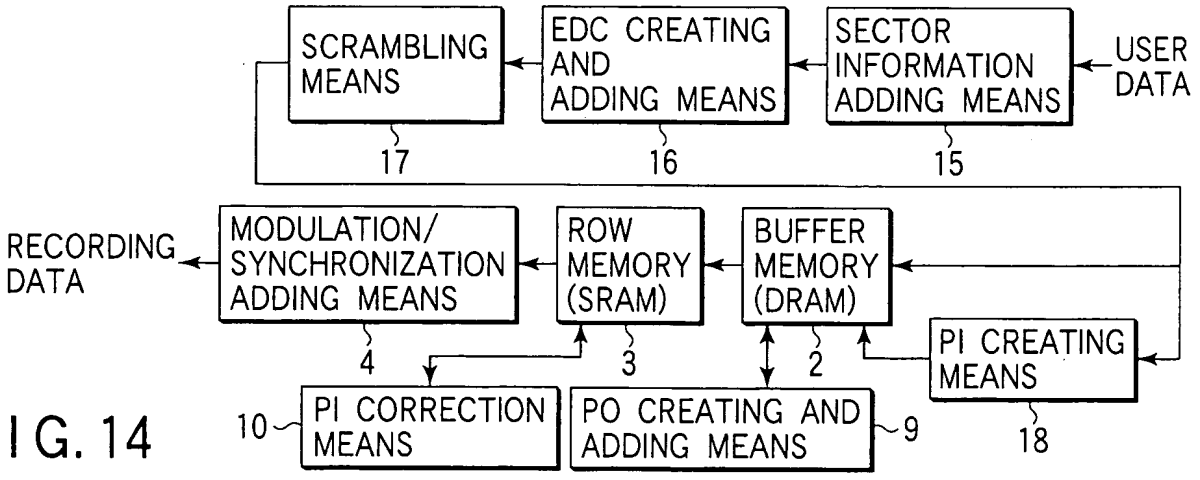

FIG. 14

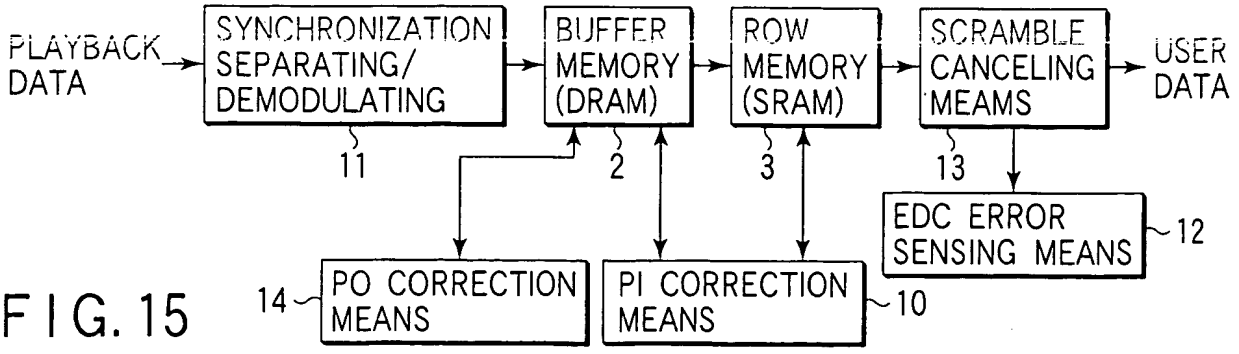

FIG. 15

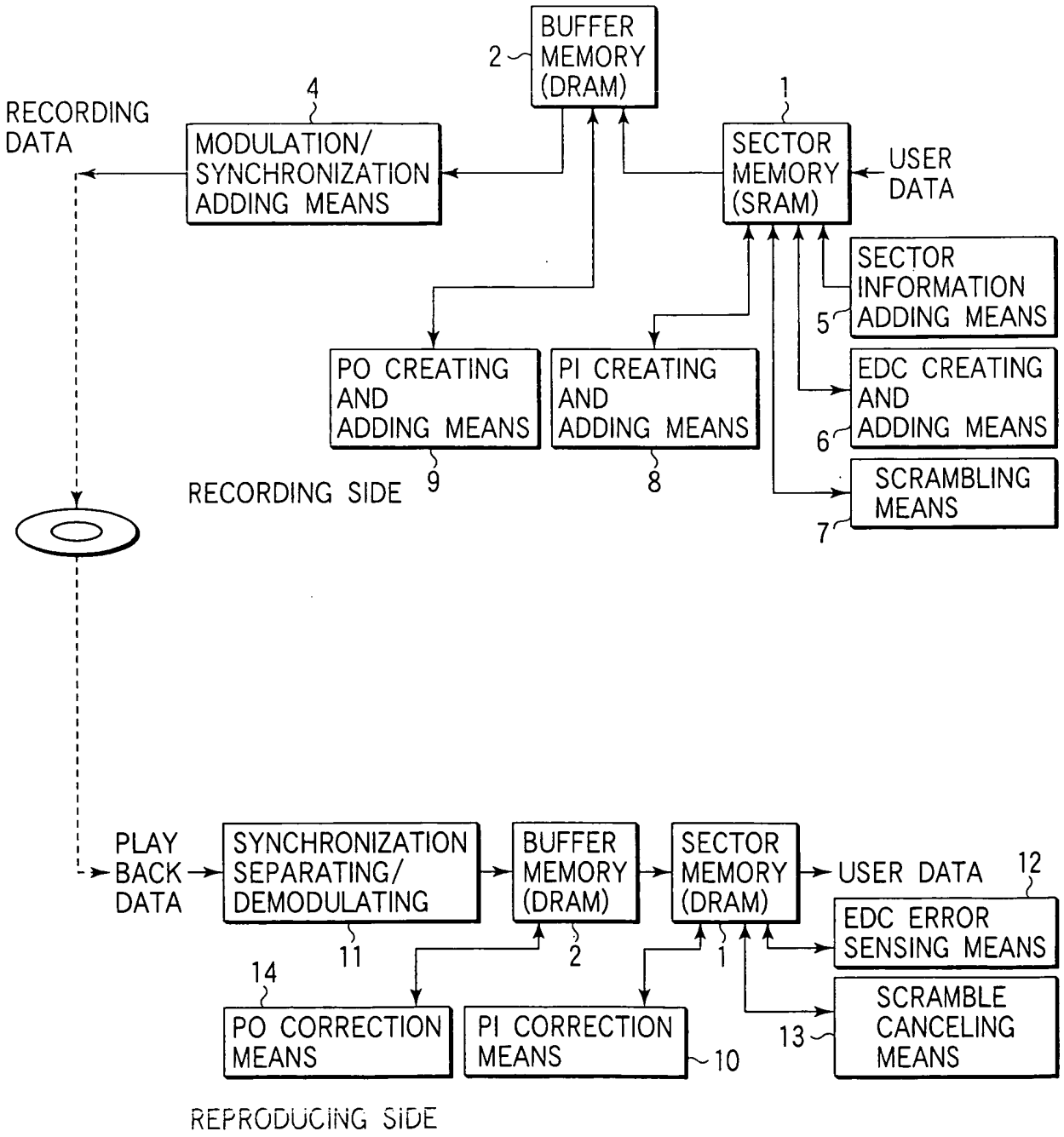
BUFFER MEMORY (DRAM)
2
4
1
RECORDING DATA
MODULATION/ SYNCHRONIZATION ADDING MEANS
SECTOR MEMORY (SRAM)
USER DATA
SECTOR INFORMATION ADDING MEANS
5
PO CREATING AND ADDING MEANS
PI CREATING AND ADDING MEANS
EDC CREATING AND ADDING MEANS
6
RECORDING SIDE
9
8
SCRAMBLING MEANS
7
PLAY BACK DATA
SYNCHRONIZATION SEPARATING/ DEMODULATING
BUFFER MEMORY (DRAM)
SECTOR MEMORY (DRAM)
USER DATA
12
EDC ERROR SENSING MEANS
11
2
1
14
PO CORRECTION MEANS
PI CORRECTION MEANS
10
13
SCRAMBLE CANCELING MEANS
REPRODUCING SIDE

FIG. 16

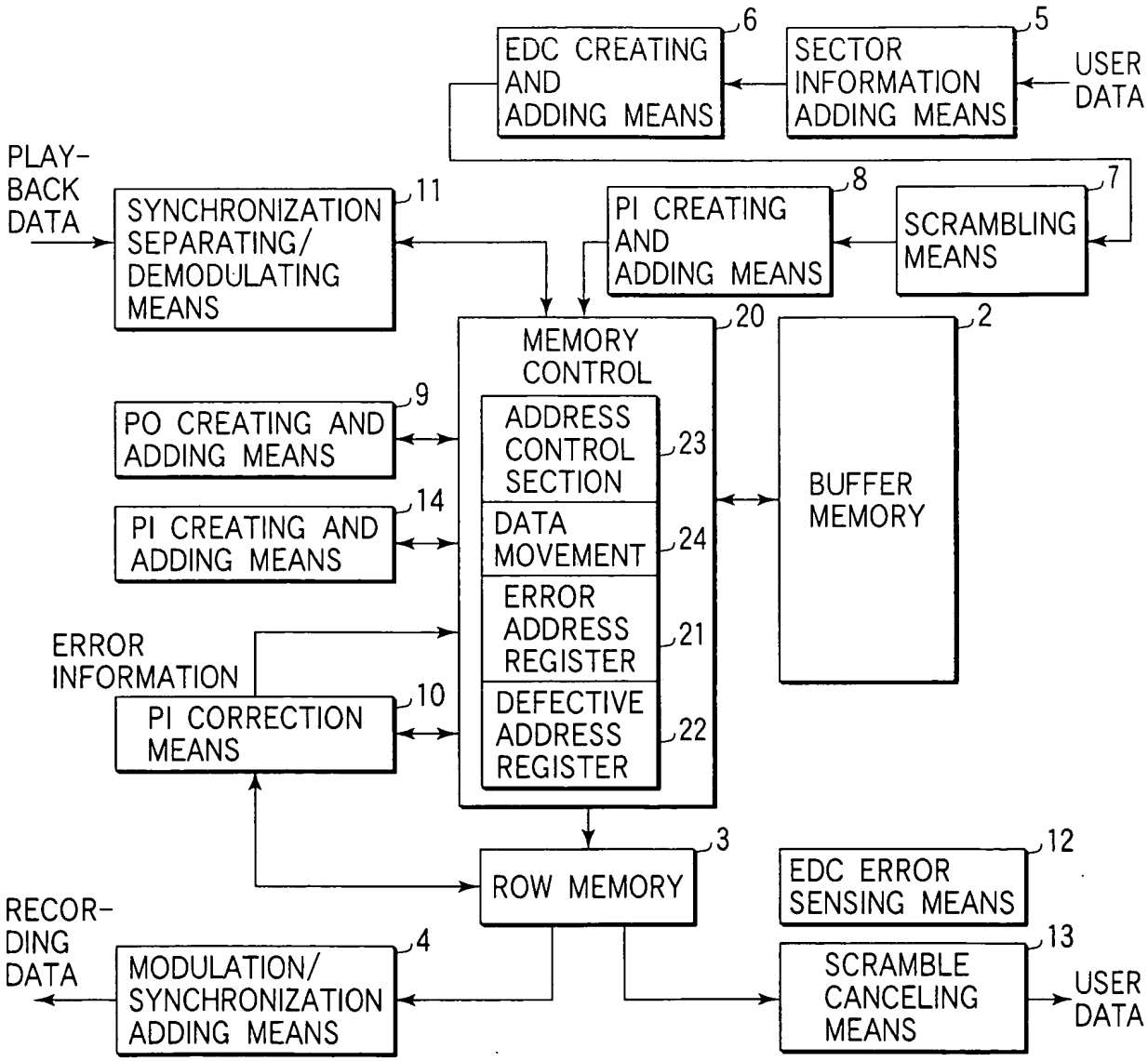
EDC CREATING AND ADDING MEANS
6
SECTOR INFORMATION ADDING MEANS
5
USER DATA
PLAY-BACK DATA
SYNCHRONIZATION SEPARATING/ DEMODULATING MEANS
11
PI CREATING AND ADDING MEANS
8
SCRAMBLING MEANS
7
MEMORY CONTROL
20
2
PO CREATING AND ADDING MEANS
9
ADDRESS CONTROL SECTION
23
BUFFER MEMORY
PI CREATING AND ADDING MEANS
14
DATA MOVEMENT
24
ERROR ADDRESS REGISTER
21
ERROR INFORMATION
PI CORRECTION MEANS
10
DEFECTIVE ADDRESS REGISTER
22
ROW MEMORY
3
EDC ERROR SENSING MEANS
12
RECOR-DING DATA
MODULATION/ SYNCHRONIZATION ADDING MEANS
4
SCRAMBLE CANCELING MEANS
13
USER DATA

FIG. 17

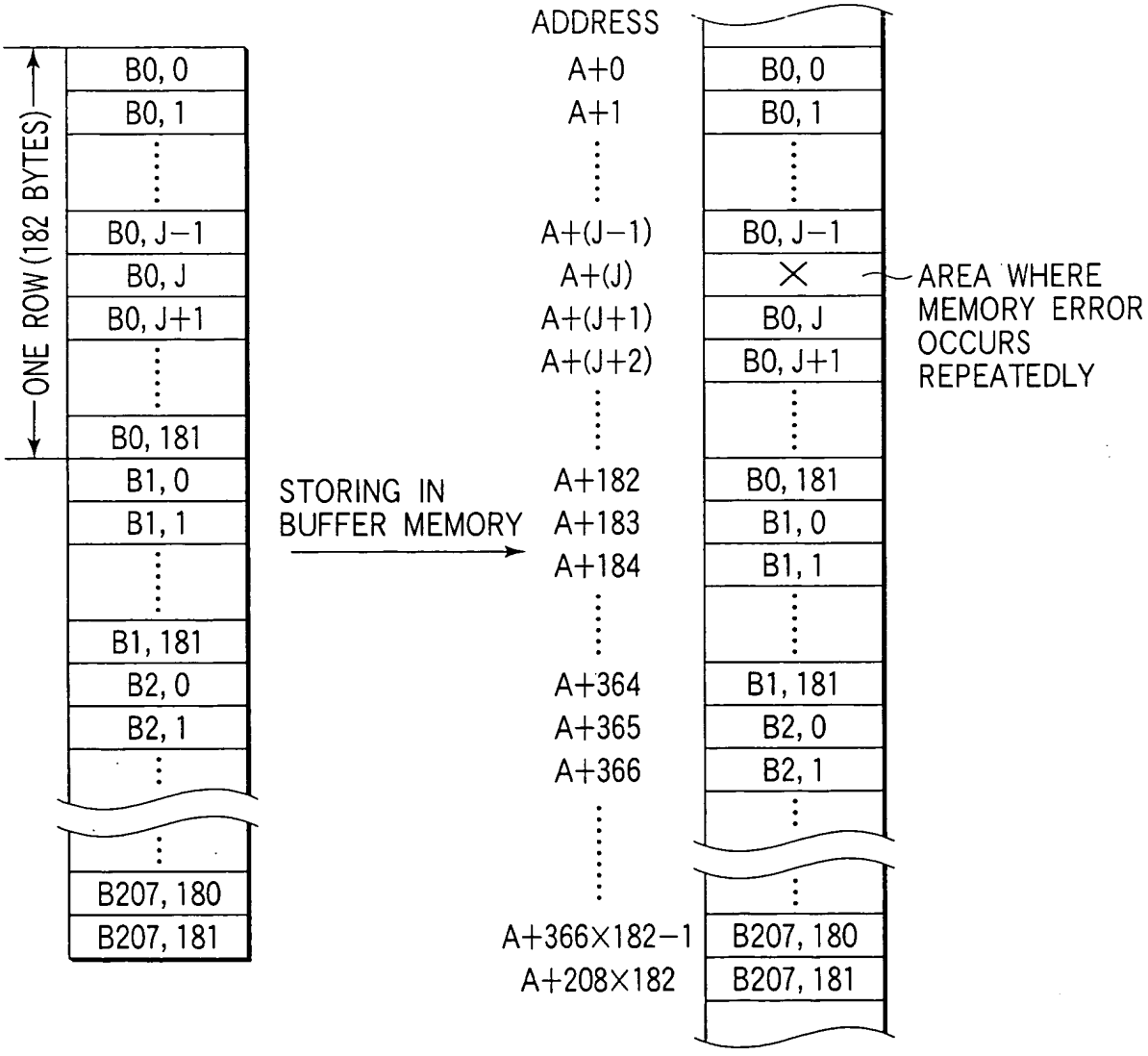

FIG. 18A

FIG. 18B

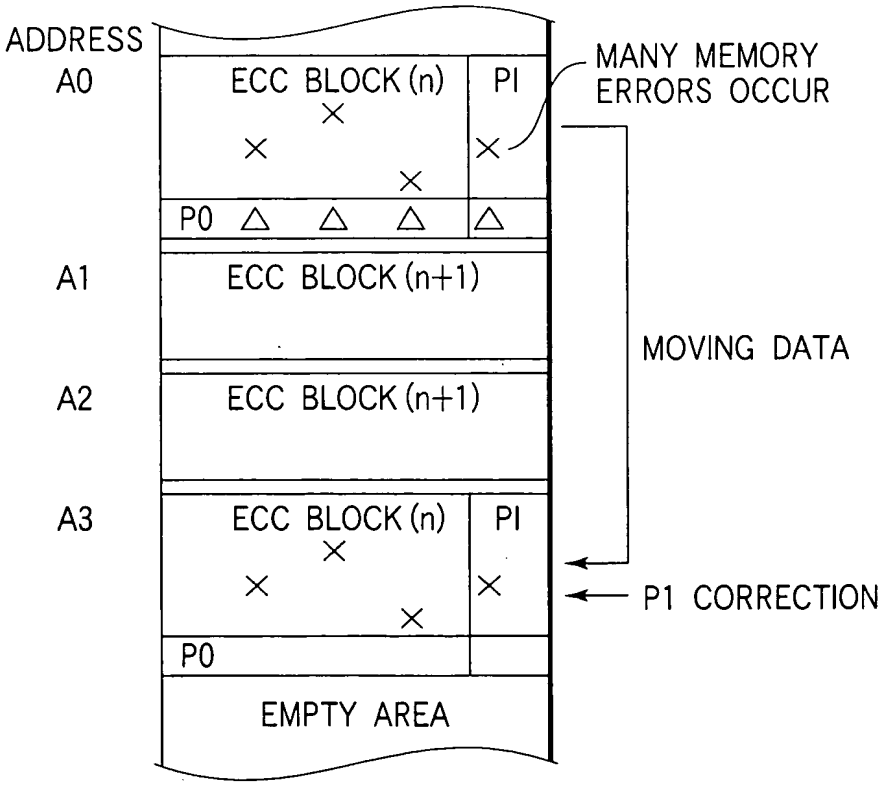
ADDRESS
A0
ECC BLOCK (n)
PI
MANY MEMORY ERRORS OCCUR
P0
A1
ECC BLOCK (n+1)
MOVING DATA
A2
ECC BLOCK (n+1)
A3
ECC BLOCK (n)
PI
P1 CORRECTION
P0
EMPTY AREA

FIG. 19